Towards green and scalable flexible electronics: R2R printed 4-bit microprocessor with SWCNT-based logic

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A microprocessor is the central component in nearly all modern electronic systems, such as smartphones, tablets, laptops, routers, servers, automobiles, and Internet of Things (IoT) devices. Although conventional Si-based technologies have enabled the widespread use of microprocessors, they face significant limitations in terms of reducing device weight (flexibility), lowering manufacturing costs, and minimizing environmental impact. Roll-to-roll (R2R) gravure printing has emerged as a promising alternative, offering high throughput, low costs, and large-area fabrication with a minimal carbon footprint and no hazardous byproducts(*1*, *2*). In this study, we present the development and demonstration of the world's first fully R2R gravure-printed flexible 4-bit microprocessor, which consists of over 1,200 thin-film transistors (TFTs) fabricated entirely through a continuous R2R process. To achieve this, we designed R2R-compatible standard cell libraries by optimizing the electrical characteristics of both *p*-type and *n*-type single-walled carbon nanotube (SWCNT)-TFTs. These libraries were essential for ensuring reliable logic operation and were validated with a process design kit (PDK), ensuring that the circuit schematics aligned with the physical layouts. Complementary logic operation was achieved by engineering the threshold voltages (V_{th}) of both transistor types through controlled doping. To minimize V_{th} variation, we used a rheological tuning method to ensure uniform topography in the printed dielectric patterns, which are particularly sensitive to such variations. To scale down the TFT geometry—including channel length and width—we developed an ensemble linear regression model to analyze registration marker superposition errors over time, allowing us to predict machine-direction (MD) errors within the R2R system. Additionally, we employed Spectre simulations integrated with artificial neural networks to facilitate rapid and variation-aware PDK generation. Following these core strategies, we successfully fabricated a flexible Harvard-architecture 4-bit processor that integrates phase A/B control, a program counter, an accumulator, a FETCH unit, register-out logic, and a 4-bit arithmetic logic unit (ALU). This work establishes a foundation for scalable, eco-friendly, and fully R2R-printed flexible computing systems.

References

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